A4945/4949

Three Phase Sensorless Fan Driver

FEATURES AND BENEFITS

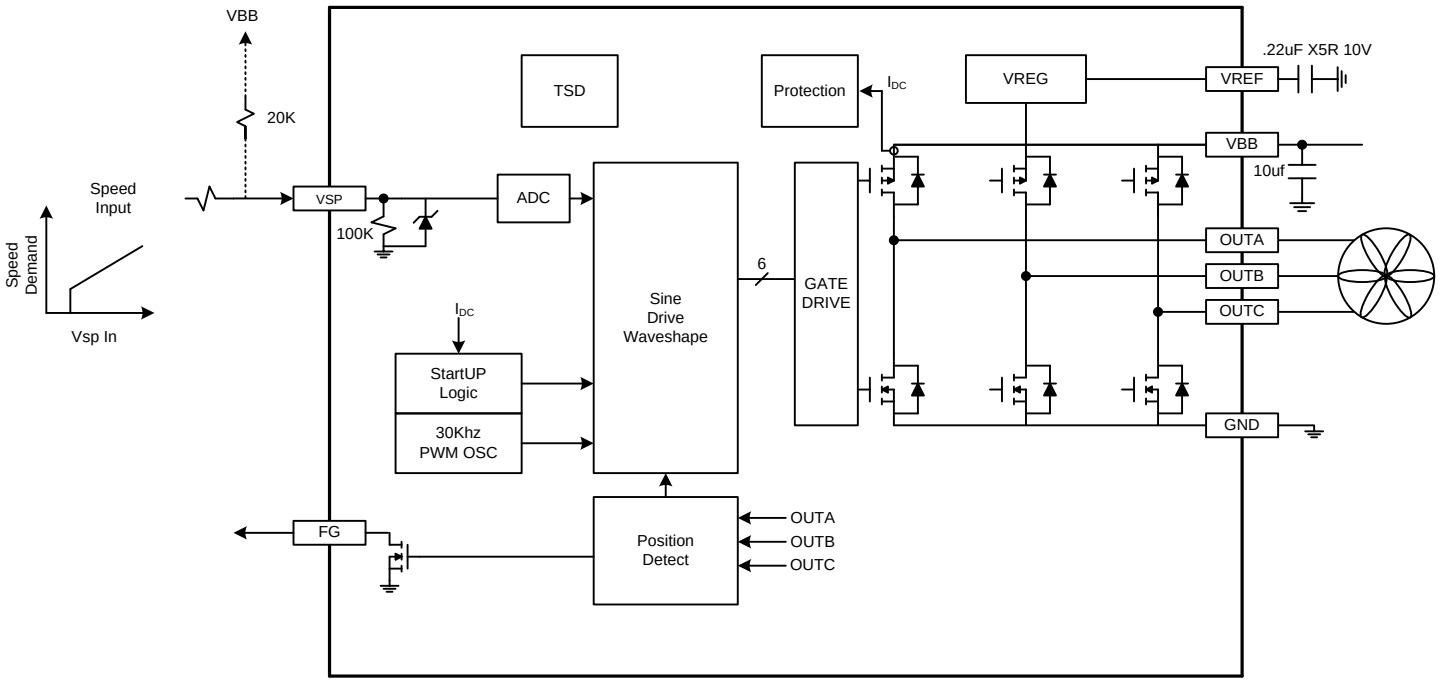
- 180 Degree Sinusoidal Drive For Low Audible Noise
- High Efficiency Control Algorithm
- Sensorless Operation
- Analog Speed Input – A4945
- PWM Speed Input – A4949
- Wide supply voltage range
- FG Speed Output
- Lock Detection
- Overcurrent Protection
- Soft Start
- Short Circuit Protection

DESCRIPTION

The A4945 and A4949 three phase motor drivers incorporate sinusoidal drive to minimize audible noise and vibration for medium power fans.

A Speed Input is provided to control motor speed. This allows system cost savings by eliminating an external variable power supply. Alternatively, power supply modulation down to 4V can be used to adjust motor speed.

The A4945 and A4949 are supplied in a 8L SOIC with exposed power pad, (suffix LJ), and 8L SOIC (suffix "L").



Typical Application (A4945)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{BB}				18	V
Input Voltage Range	V_{IN}	VSP/PWM	-.3		VBB	V
Logic Output	Vo	FG			18	V
Output Current	I_{OUT}	Internally Limited			I_{OCLMAX}	A
Junction Temperature	Tj				150	°C
Storage Temperature Range	Ts		-55		150	°C
Operating Temperature Range	Ta		-40		105	°C
Package Thermal Resistance						
LJ package	Rja	2 sided PCB 1 in^2 Copper		40		°C/W
L package		2 sided PCB 1 in^2 Copper		120		°C/W

A4945 TERMINAL LIST

Pin Name	Pin Description	Num
GND	Ground	1
OUTA	Motor Terminal	2
VBB	Input Supply	3
VSP	Logic Input – Speed	4
VREF	Analog Output	5
FG	Speed Output Signal	6
OUTC	Motor Terminal	7
OUTB	Motor Terminal	8

A4949 TERMINAL LIST

Pin Name	Pin Description	Num
GND	Ground	1
OUTA	Motor Terminal	2
VBB	Input Supply	3
PWM	Logic Input – Speed	4
VREF	Analog Output	5
FG	Speed Output Signal	6
OUTC	Motor Terminal	7
OUTB	Motor Terminal	8

ELECTRICAL CHARACTERISTICS at T_A = +25°C, VBB = 4V to 18V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
VBB Supply Current	I_{BB}	VSP=3V		10	tbd	mA
Total Driver Rdson (Sink + Source)	R_{DSON}	I = 1A, Tj=25C, VBB=12V		tbd		Ohm
		I = 1A, Tj=25C, VBB=4V		tbd		Ohm
		Source Driver		tbd		Ohm
		Sink Driver		Tbd		Ohm
VREF	V_{REF}	I_{OUT}=5mA	3.2	3.3	3.4	V
Input Current (PWM/VSP pin)	Iin	Vin = 3V (100K pulldown)	21	33	45	uA
Output Sat Voltage	V_{SAT}	I=5mA			.3	V
FG Output Leakage	I_{FG}	V=18V			1	uA
A4945 Speed Input						
VSP Awake Threshold Level	VTH_{AWK}		.6	.9	1.2	V
VSP Awake Time	T_{AWK}	C_{VREF}=1uF	100			uS
VSP Disable Threshold	VTH_{STB}		194	228	264	mV
VSP Accuracy				+/- 6LSB		
VSP Maximum Level			2.95	3	3.05	
A4949 Speed Input						
PWM On Threshold	DC_{ON}			10		%
PWM Off Threshold	DC_{OFF}			7.5		%
PWM Input Frequency Range	F_{PWM}		.1		100	Khz
Motor PWM Frequency	Fpwm		28	30	32	kHz
VBB UVLO	VBB_{UVLO}	VBB rising		3.85	3.98	V
VBB UVLO HYS	VBB_{HYS}		150	300	450	mV
Lock Protection	t_{OFF}		7	8	9	S
Overcurrent	I_{OCL}		1.4	1.6	1.8	A
Thermal Shutdown Temp.	T_{JTSD}	Temperature increasing.	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = T_{JTSD} - ΔT_J		20		°C

1. Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

Functional Description

The A4945/A4949 targets fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds. The trapezoidal startup method does not require any external components and will automatically switch to sinusoidal operation as the motor is accelerating up to operating speed.

The speed of the fan can be controlled by voltage mode (control of power supply amplitude), variable duty cycle PWM input (A4949), or via an adjustable analog input (A4945). Use of the PWM or analog input allows overall system cost savings by eliminating the requirement of an external variable power supply. Operation down to 4V can be achieved to allow the IC to fit into legacy systems with voltage mode operation.

The speed input (duty or Vin) is measured and converted to a 9bit number. This 9 bit "demand" is applied to a pwm generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120 degree phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

A bemf detection "window" is opened on phase A modulation profile in order to measure the rotor position so as to define the modulation timing. The control system maintains the window to a small level in order to minimize the disturbance and approximate the ideal sinusoidal current waveform as much as possible.

A Soft start feature is integrated to minimize demand on the power supply at startup and smoothly initiate motor rotation.

Protection features include lock detection with restart, overcurrent limit, motor output short circuit, supply undervoltage monitor and thermal shutdown.

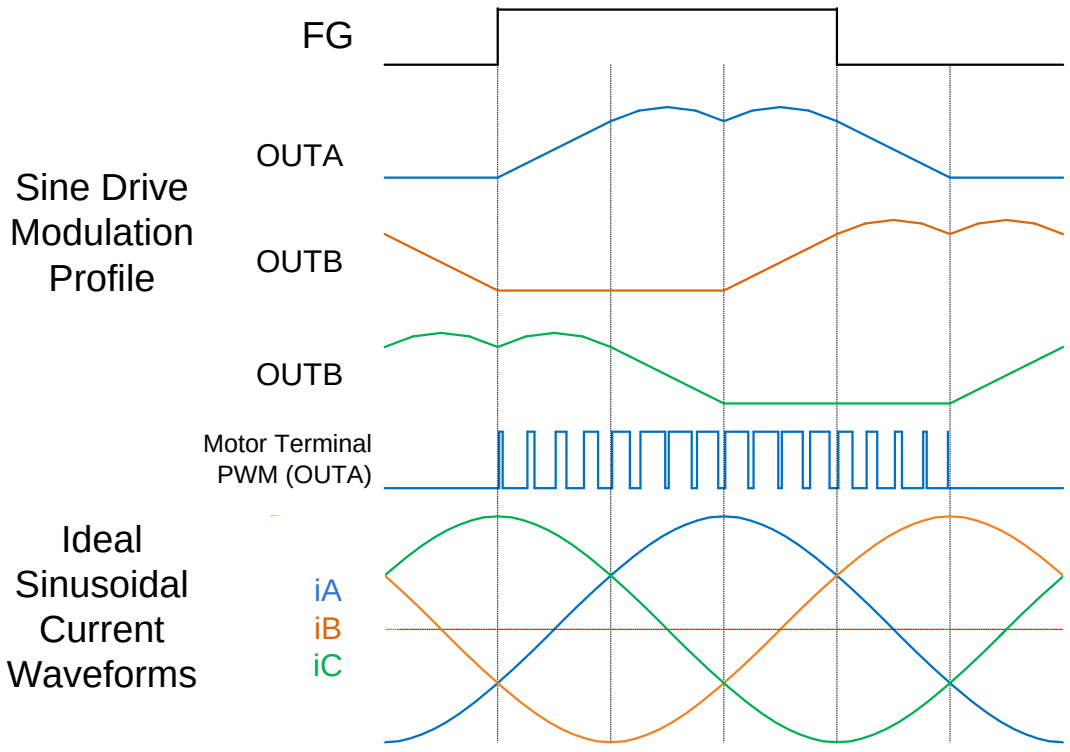


Figure 1: Sinusoidal PWM

Speed Control.

A4945 – VSP - Analog Input. An internal ADC translates the input voltage to a demand value to control speed of the fan. The motor drive will be disabled if VSP is lower than VTH_{DIS}. Upon startup, VSP must exceed VTH_{AWK} for T_{AWK}. The T_{AWK} delay is required to allow internal reference supply and analog circuits to properly power up. After this short delay, VIN can be adjusted below VTH_{AWK} to allow full scale operation (7.5% to 100%).

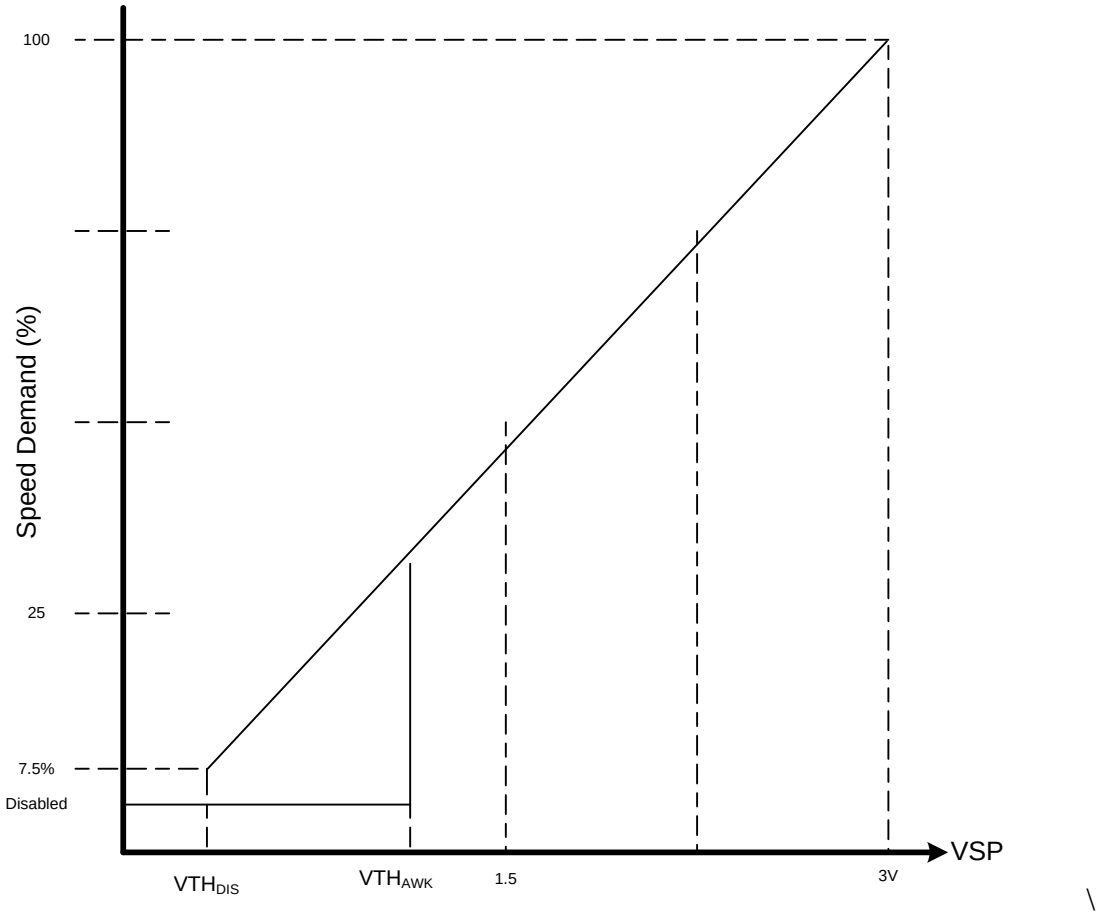


Figure 2) A4945 Speed Input Characteristic

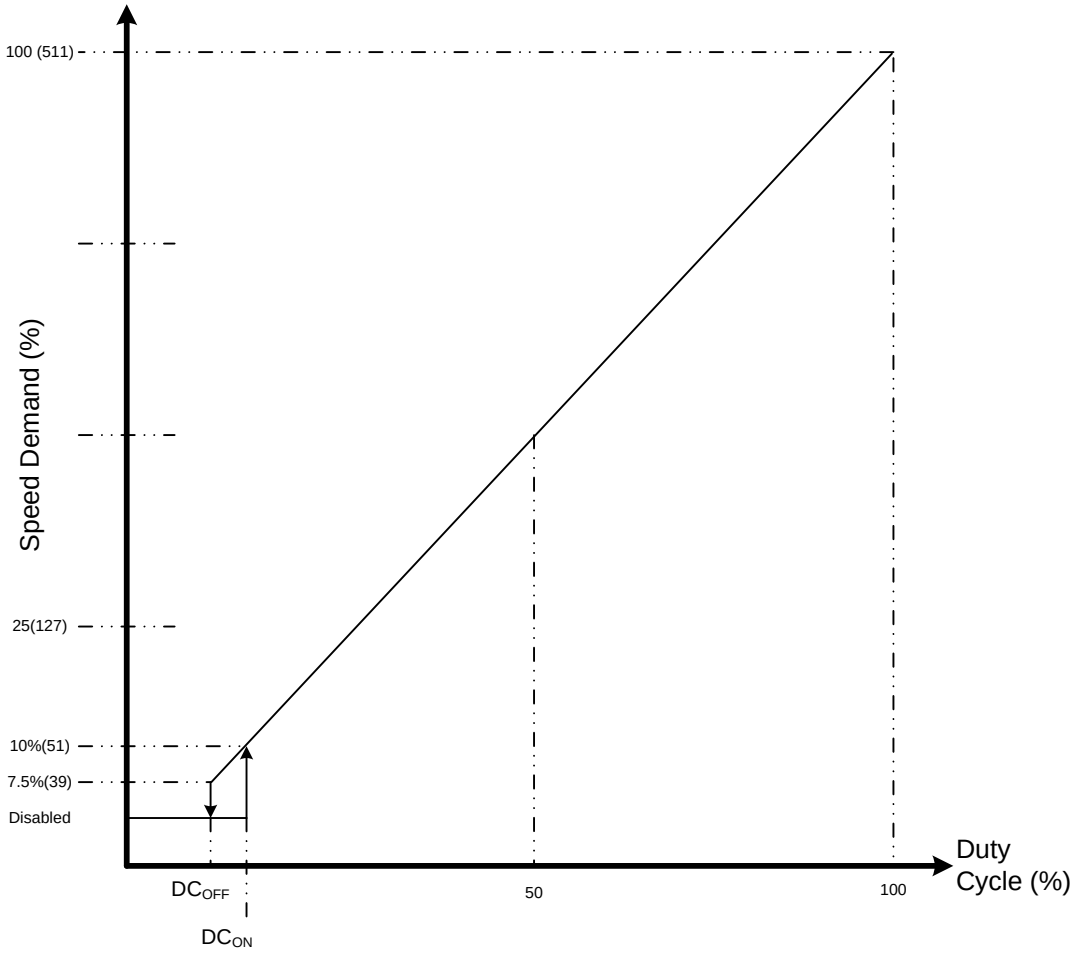
Speed Control (continued).

A4949 – PWM – Duty Cycle Input. An digital duty cycle measurement circuit converts the applied duty to to a demand value (9 bit resolution) to control speed of the fan.

The motor drive will be enabled if duty is larger than DC_ON (typically 10%). The PWM input is filtered to prevent spurious noise from turning on or off unexpectedly.

There is an internal pulldown (100K) that will turn motor off if input signal is disconnected. If 100% speed demand is desired for Open PWM condition, connect a 10K pullup resistor to VREF pin.

Power Supply Modulation. Speed can be controlled simply by varying the power supply voltage. To allow this function, insert a 20K pullup from VSP(4945) or PWM(4949) to VBB. Motor Drive will be enabled and disabled at undervoltage rising and falling thresholds.



Duty Cycle IN (Fpwm = 100Hz to 100Khz)

Figure 3) A4949 Speed Input Characteristic

Lock Detect. Speed is monitored to determine if rotor is locked. If a lock condition is detected, the IC will be disabled for T_{OFF} an auto-restart is attempted.

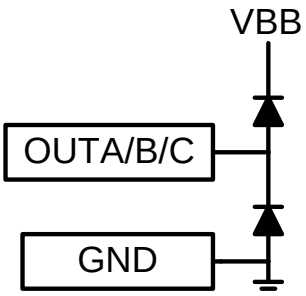
FG. Open drain output provides speed information to the system. FG changes state one period per electrical revolution of the motor (as shown in Figure 1).

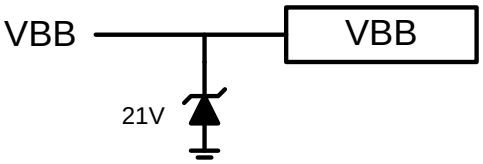
Current Limit. During a locked rotor condition the current can ramp up to the internal current limit. Load Current is monitored on the high side MOSFET. If the current has reached $I_{OCL,}$ the source drivers will turn off for the remaining time of the PWM cycle.

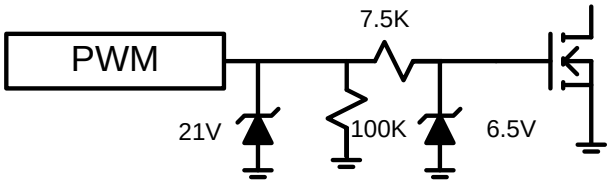
Application Information

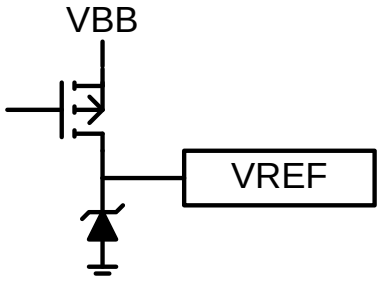
Layout Notes

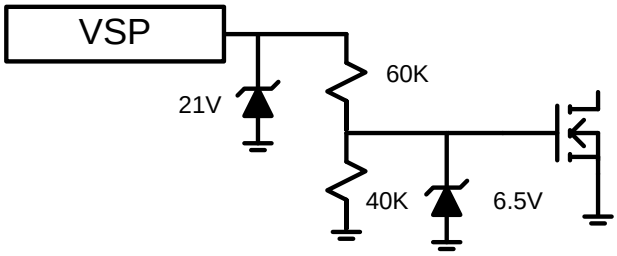
Pin Diagrams

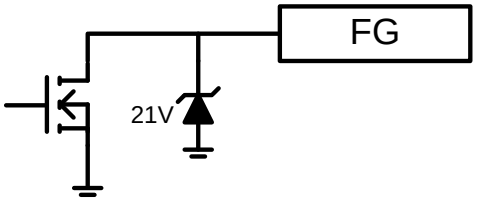




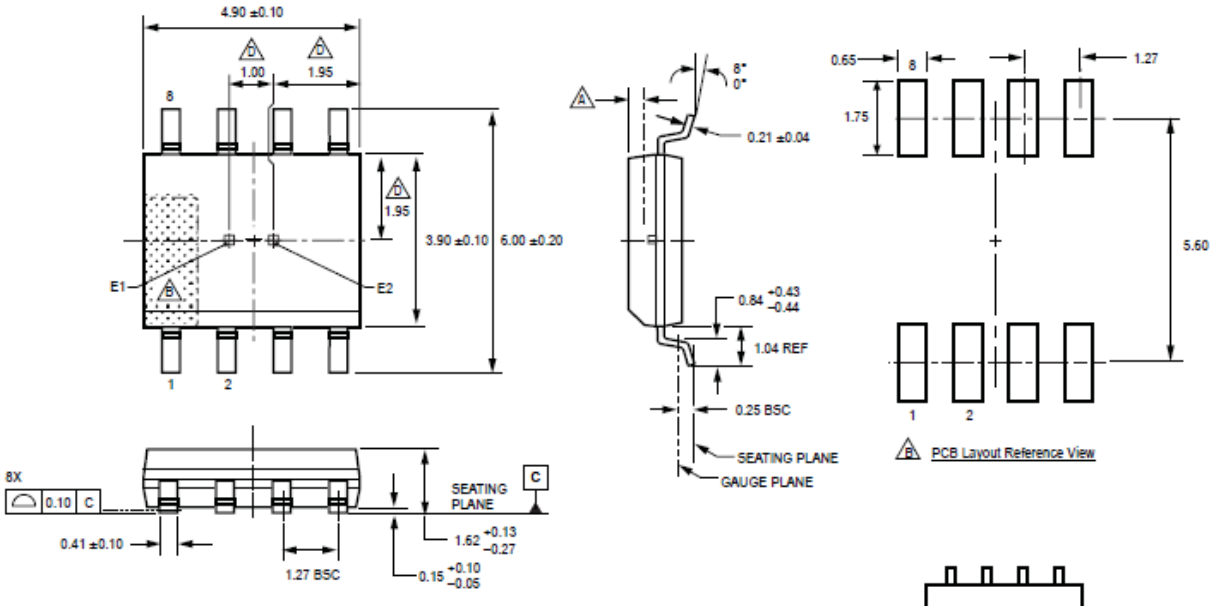








Package L, 8-pin SOICN



For Reference Only; not for tooling use (reference DWG-9204)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Active Area Depth, 0.40 mm REF

B Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Terminal #1 mark area

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

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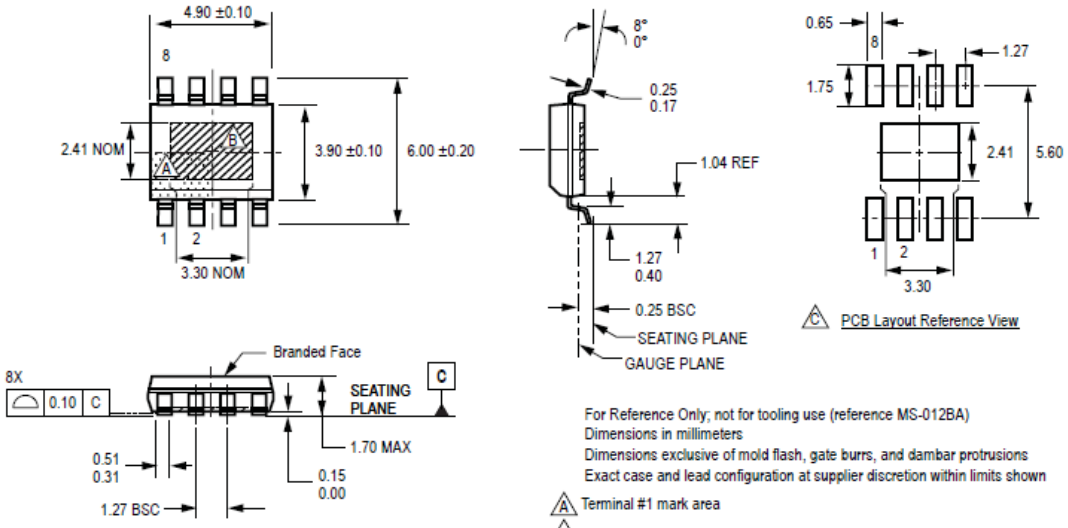
Package LJ, 8 Pin SOIC



For Reference Only; not for tooling use (reference MS-012BA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)